CLAIMS:

1. A method of operating a network device, comprising:

receiving electronic data from a first port of the data networking device;

deleting at least a portion of the electronic data prior to providing the electronic data to the memory of the networking device;

providing at least a portion of the electronic data to a second port.

2. The method of claim 1, further comprising modifying the electronic data prior to said providing.

3. The method of claim 1, wherein the electronic data comprise a frame.

4. The method of claim 1, wherein the portion of electronic data deleted comprises a VLAN (virtual local area network) tag.

5. The method of claim 3, wherein modifying comprises inserting a VLAN tag to the frame.

6. The method of claim 3, further comprising generating a CRC (cyclic redundancy code) and inserting the CRC into the frame prior to providing to the memory.

7. The method of claim 1, further comprising providing a portion of the electronic data to a control module prior to deleting a portion of the electronic data.

8. The method of claim 7, wherein the portion of data provided to the control module comprises the protocol header.

9. The method of claim 1, wherein the first port and the second port comprise a receive port and a transmit port, respectively.

10. An apparatus, comprising:

one or more receive ports capable of receiving electronic data from a network;

one or more transmit ports capable of transmitting electronic data to a network;

a memory; and

a processor, the processor configured to, in operation:

delete at least a portion of the electronic data received by the one or more receive ports;

provide the remaining electronic data to the memory;

read the electronic data from the memory;

modify the electronic data after reading from the memory; and

provide at least a portion of the electronic data to one or more of the transmit ports.

11. The apparatus of claim 10, wherein the processor is further configured to modify the electronic data prior to providing at least a portion of the electronic data to one or more of the transmit ports.

12. The apparatus of claim 10, wherein the apparatus comprises a network switch.

13. The apparatus of claim 12, wherein said memory comprises network switch internal memory.

14. The apparatus of claim 10, wherein said portion of electronic data deleted substantially comprises a VLAN tag.

15. The apparatus of claim 11, wherein modifying the electronic data comprises inserting a VLAN tag, wherein the VLAN tag relates at least in part to the destination address of the electronic data.

16. The apparatus of claim 10, wherein the processor comprises a network processor.

17. The apparatus of claim 10, wherein the memory comprises a plurality of memory devices.

18. The apparatus of claim 17, wherein the plurality of memory devices comprise one or more of: random access memory, static random access memory, and synchronous dynamic random access memory.

19. A system for network data communication, comprising:

a first port to receive electronic data from a network;

a second port to transmit electronic data to a network;

a memory to store electronic data; and

a processor coupled to the first port, second port, and the memory, wherein the processor is configured to, in operation, delete at least a portion of electronic data received on a first port, provide at least a portion of the electronic data to the memory, and modify the electronic data prior to providing at least a portion of the electronic data to the second port.

20. The system of claim 19, wherein the electronic data comprise a frame.

21. The system of claim 19, wherein the portion of electronic data deleted comprises a VLAN (virtual local area network) tag.

22. The system of claim 20, further comprising generating a CRC (cyclic redundancy code) and inserting the CRC into the frame prior to providing to the memory.

23. The system of claim 19, wherein modifying the electronic data comprises inserting a VLAN tag, wherein the VLAN tag relates at least in part to the destination address of the electronic data.

24. The system of claim 19, wherein the processor comprises a network processor.

25. The system of claim 19, wherein the memory comprises a plurality of memory devices.

26. The system of claim 25, wherein the plurality of memory devices comprise one or more of: random access memory, static random access memory, and synchronous dynamic random access memory.

27. The system of claim 19, wherein said processor is configured to modify said electronic data only if said second port is configured to recognize tags.